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for

METHOD AND APPARATUS FOR CONTROLLING A DUAL-SLOPE INTEGRATOR CIRCUIT TO ELIMINATE SETTLING TIME EFFECT

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METHOD AND APPARATUS FOR CONTROLLING A DUAL-SLOPE INTEGRATOR CIRCUIT TO ELIMINATE SETTLING TIME EFFECT

CROSS-REFERENCE TO RELATED APPLICATION

This application claims priority of Taiwanese application no. 092120536, filed on July 28, 2003.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to a method and apparatus for controlling a dual-slope integrator circuit, more particularly to a method and apparatus for controlling a dual-slope integrator circuit to eliminate settling time effect.

2. Description of the Related Art

Conventional dual-slope integrators are widely used in linear systems, such as analog-to-digital conversion, time interval measurement, etc. Referring to Figure 1, a conventional dual-slope integrator 1 is shown to include an operational amplifier 10. As shown in Figure 2, in operation, the dual-slope integrator 1 generally requires a settling time (T_S) before reaching a linear operating region (T_L) during which a stable output can be obtained from the operational amplifier 10. As such, as shown in Figure 3, in a time interval measuring device 11, a control circuit 12 is used in controlling the dual-slope integrator 1 to eliminate the settling time effect. In this configuration, a digital clock signal and an analog input test signal must be inputted to the

control circuit 12 for synchronization. However, the high-frequency digital clock signal can interfere with the analog input test signal and cannot be easily synchronized with the latter. In U.S. Patent No. 6,137,749, there is disclosed a control circuit constructed from a finite state machine so as to solve the aforesaid synchronization problem between the digital clock signal and the analog input test signal. However, the control circuit proposed in the aforesaid patent is not only large and complicated, but also does not address the problems associated with the settling time of the dual-slope integrator and interference between the digital clock signal and the analog input test signal.

SUMMARY OF THE INVENTION

Therefore, the object of the present invention is to provide a method and apparatus for controlling a dual-slope integrator circuit so as to solve the above drawbacks associated with the prior art.

According to one aspect of the present invention, there is provided a method for controlling a dual-slope integrator circuit. The integrator circuit has an integrating capacitor, a reset input for receiving a reset signal that is used in maintaining a reset state of the integrating capacitor, and an integrator input for receiving a signal to be integrated. The method comprises the steps of:

a) in response to an original input signal, generating the reset signal that is provided to the reset input and that has a predetermined reset time period;

b) simultaneous with step a), generating a delayed input signal by introducing a predetermined delay period into the original input signal, the delay period being longer than the reset time period; and

c) with reference to the original input signal and the delayed input signal, generating a trigger signal that is provided to the integrator input for enabling charging operation of the integrating capacitor during a charging period that starts from the end of the reset time period and that terminates at a lagging edge of the delayed input signal.

According to another aspect of the present invention, there is provided a method for controlling a dual-slope integrator circuit. The integrator circuit has an integrating capacitor, a reset input for receiving a reset signal that is used in maintaining a reset state of the integrating capacitor, and an integrator input for receiving a signal to be integrated. The method comprises the steps of:

a) in response to an original input signal, generating a trigger signal that is provided to the integrator input;

b) simultaneous with step a), generating the reset signal that is provided to the reset input and that has a predetermined reset time period such that charging

operation of the integrating capacitor is enabled only at the end of the reset time period;

c) simultaneous with step a), generating a delayed input signal by introducing a predetermined delay period into the original input signal, the delay period being longer than the reset time period; and

d) terminating generation of the trigger signal upon detection of a lagging edge of the delayed input signal.

According to yet another aspect of the present invention, there is provided an apparatus for controlling a dual-slope integrator circuit. The integrator circuit has an integrating capacitor, a reset input for receiving a reset signal that is used in maintaining a reset state of the integrating capacitor, and an integrator input for receiving a signal to be integrated. The apparatus comprises a one-shot circuit, a delay circuit, and a control circuit. The one-shot circuit is adapted to receive an original input signal and to generate the reset signal, that is provided to the reset input and that has a predetermined reset time period, in response to the original input signal. The delay circuit is adapted to receive the original input signal and to generate a delayed input signal by introducing a predetermined delay period into the original input signal, the delay period being longer than the reset time period. The control circuit is adapted to receive the original input signal and the delayed

input signal and to generate a trigger signal that is provided to the integrator input for enabling charging operation of the integrating capacitor during a charging period that starts from the end of the reset time period and that terminates at a lagging edge of the delayed input signal.

According to a further aspect of the present invention, there is provided an apparatus for controlling a dual-slope integrator circuit. The integrator circuit has an integrating capacitor, a reset input for receiving a reset signal that is used in maintaining a reset state of the integrating capacitor, and an integrator input for receiving a signal to be integrated. The apparatus comprises a control circuit, a one-shot circuit, and a delay circuit. The control circuit is adapted to receive an original input signal and to generate a trigger signal, that is provided to the integrator input, in response to the original input signal. The one-shot circuit is adapted to receive the original input signal and to generate the reset signal, that is provided to the reset input and that has a predetermined reset time period, in response to the original input signal. Charging operation of the integrating capacitor is enabled by the one-shot circuit only at the end of the reset time period. The delay circuit is adapted to receive the original input signal and to generate a delayed input signal by introducing a predetermined delay period into

the original input signal, the delay period being longer than the reset time period. The control circuit is coupled to the delay circuit so as to receive the delayed input signal therefrom, and terminates generation of the trigger signal upon detection of a lagging edge of the delayed input signal.

BRIEF DESCRIPTION OF THE DRAWINGS

Other features and advantages of the present invention will become apparent in the following detailed description of the preferred embodiment with reference to the accompanying drawings, of which:

Figure 1 illustrates a conventional dual-slope integrator;

Figure 2 illustrates an output waveform of the conventional dual-slope integrator;

Figure 3 is a block diagram of a conventional time interval measuring device;

Figure 4 is a circuit diagram of the preferred embodiment of an apparatus for controlling a dual-slope integrator circuit according to the present invention; and

Figures 5A to 5F illustrate exemplary waveforms of an original input signal, a reset signal, a delayed input signal, a trigger signal, a latch output signal, and an integrator output signal generated in the circuit of Figure 4.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Figure 4 illustrates the preferred embodiment of an apparatus 2 for controlling a dual-slope integrator circuit 3 to eliminate settling time effect according to the present invention. The integrator circuit 3 includes an operational amplifier 31, a first resistor 32, a second resistor 33, a slope control switch 34, an integrating capacitor 35, and a reset switch 36. The integrator circuit 3 further has a reset input for receiving a reset signal 41 that is used in controlling ON/OFF states of the reset switch 36 for controlling in turn a reset state of the integrating capacitor 35, an integrator input for receiving a signal 43 to be integrated, and an integrator output from which an integrator output signal (Vo) is obtained. The first resistor 32 has one end for receiving the signal 43, and another end connected to an inverting input of the operational amplifier 31. The second resistor 33 has one end for receiving the signal 43 through the slope control switch 34, and another end connected to the inverting input of the operational amplifier 31. The integrating capacitor 35 has one end connected to the inverting input of the operational amplifier 31, and another end connected to the output of the operational amplifier 31. The operational amplifier 31 further has a non-inverting input for receiving a reference voltage (Vref).

The apparatus 2 includes a one-shot circuit 21, a delay circuit 22, and a control circuit 25.

The one-shot circuit 21 is adapted to receive an original input signal 40 (see Figure 5A), which is a pulse signal, and to generate the reset signal 41 (see Figure 5B), that is provided to the reset input of the integrator circuit 3 for closing the reset switch 36 and that has a predetermined reset time period (Tz), in response to the original input signal 40. The integrating capacitor 35 is thus short-circuited by the reset switch 36 to maintain a reset state of the integrating capacitor 35 during the reset time period (Tz). Hence, the integrator output signal (Vo) (see Figure 5F) is equal to the reference voltage (Vref) during the reset time period (Tz). The reset time period (Tz) is longer than a measured settling time (Ts) of the integrator circuit 3. At the end of the reset time period (Tz), the reset switch 36 is opened so that charging of the integrating capacitor 35 becomes possible.

The delay circuit 22 is adapted to receive the original input signal 40 and to generate a delayed input signal 40' (see Figure 5C) by introducing a predetermined delay period (Td) into the original input signal 40. The delay period (Td) is longer than the reset time period (Tz) by a duration not smaller than the measured settling time (Ts) of the integrator circuit 3.

The control circuit 25 is adapted to receive the original input signal 40 and the delayed input signal 40' and to generate a trigger signal 43 (see Figure 5D) that is provided to the integrator input of the integrator circuit 3 for enabling charging operation of the integrating capacitor 35 during a charging period that starts from the end of the reset time period (Tz) and that terminates at a lagging edge of the delayed input signal 40'. In this embodiment, the control circuit 25 includes an SR latch 23 and a logic NOR gate 24.

The SR latch 23 has a set terminal that serves as a first input terminal for receiving the original input signal 40, a reset terminal that serves as a second input terminal for receiving the delayed input signal 40', and an output terminal from which a latch output signal 42 (see Figure 5E) is obtained.

The logic NOR gate 24 has a first input terminal for receiving the delayed input signal 40', a second input terminal coupled to the output terminal of the SR latch 23, and an output terminal from which the trigger signal 43 is obtained.

Accordingly, the control circuit 25 generates the trigger signal 43 starting from a leading edge of the original input signal 40 and terminating at the lagging edge of the delayed input signal 40'.

The method for controlling the dual-slope integrator circuit 3 according to the present invention comprises

the following steps:

a) In response to the original input signal 40 (see Figure 5A), the one-shot circuit 21 generates the reset signal 41 (see Figure 5B) that is provided to the reset input of the integrator circuit 3 and that has a predetermined reset time period (Tz). The duration of the reset time period (Tz) must be longer than the settling time (Ts) of the integrator circuit 3. Due to the reset signal 41, the reset switch 36 short-circuits the integrating capacitor 35 during the reset time period (Tz) to disable charging operation of the integrating capacitor 35.

b) Simultaneous with step a), the delay circuit 22 generates the delayed input signal 40' (see Figure 5C) by introducing a predetermined delay period (Td), which is longer than the reset time period (Tz) by a duration not smaller than the measured settling time (Ts) of the integrator circuit 3, into the original input signal 40.

c) Simultaneous with step a), since the original input signal 40 is received by the set terminal of the SR latch 23, since the delayed input signal 40' is received by the reset terminal of the SR latch 23, and since the delayed input signal 40' and the latch output signal 42 (see Figure 5E) from the SR latch 23 are received by the logic NOR gate 24, the trigger signal 43 (see Figure 5D) generated by the logic NOR gate 24 and provided

to the integrator input of the integrator circuit 3 is a low logic signal having a duration (T_2) that starts from the leading edge of the original input signal 40 and that terminates at the lagging edge of the delayed input signal 40'.

As mentioned hereinabove, charging operation of the integrating capacitor 35 is not permitted by the reset switch 36 during the reset time period (Tz). However, at the end of the reset time period (Tz), the low-logic trigger signal 43 (i.e., the potential of which is lower than the reference voltage (Vref)) enables charging of the integrating capacitor 35 through a parallel combination of the first and second resistors 33, 34 (i.e., the low-logic trigger signal 43 closes the slope control switch 34) during a charging period that starts from the end of the reset time period (Tz) and that terminates at the lagging edge of the delayed input signal 40'. As shown in Figure 5E, the charging period includes a pre-charging sub-period (T_3) that starts from the end of the reset time period (Tz) and that terminates at a leading edge of the delayed input signal 40', and an actual integrating sub-period (T_4) that follows the pre-charging sub-period (T_3) and that has a duration equal to that of the original input signal 40. The pre-charging sub-period (T_3) serves as a buffer period that is sufficient to ensure that the integrator circuit 3 has already settled down before the start of the actual

integrating sub-period (T_4) for integrating the delayed input signal 40'. It is noted herein that the effect of charges that were accumulated in the integrating capacitor 35 during the pre-charging sub-period (T_3) may be subsequently removed through appropriate calibration techniques that are well known in the art.

Thereafter, at the end of the charging period, the trigger signal 43 reverts to a high logic state (i.e., the potential thereof is predetermined to be higher than the reference voltage (Vref)). At this time, the integrating capacitor 35 of the integrator circuit 3 starts to discharge through the first resistor 32 (i.e., the high-logic trigger signal 43 opens the slope control switch 34). The integrating operation of the integrator circuit 3 for integrating the original input signal 40 is thus completed.

In sum, this invention provides a method and apparatus for controlling a dual-slope integrator circuit to eliminate settling time effect without the need for an input digital clock signal and a complicated finite-state control circuit, thereby further eliminating the problems of synchronization and cross-talk. Manufacturing costs can thus be reduced, and reliability can be enhanced in view of improved linearity of the dual-slope integrator circuit.

While the present invention has been described in connection with what is considered the most practical

and preferred embodiment, it is understood that this invention is not limited to the disclosed embodiment but is intended to cover various arrangements included within the spirit and scope of the broadest interpretation so as to encompass all such modifications and equivalent arrangements.